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09/556,473	04/21/2000	Michael Andrew Mang	0100.0000610	6795

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EXAMINER	
LI, AIMEE J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/556,473	Applicant(s) MANG ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2000 and 21 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Change of Address as received on 21 July 2000.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 16 is objected to because of the following informalities: Please correct the phrase "at least one additional thread of the plurality of threads subsequent to combing the first set of operands" in claim 16 on page 59, lines 26-27 to read "at least one additional thread of the plurality of threads subsequent to combining the first set of operands". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10 and 12-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al., U.S. Patent Number 6,446,193 (herein referred to as Alidina) in view of Wilson, U.S. Patent Number 5,896,517 (herein referred to as Wilson).

7. Referring to claim 1, Alidina has taught a multi-thread accumulation circuit that supports a plurality of threads, comprising:

a. A first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads, wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. A plurality of accumulation registers operably coupled to the first operation unit, wherein each accumulation register of the plurality of accumulation registers corresponds to one of the plurality of threads (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30)

c. A selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers (Alidina column 4, lines 63-66 and Figure 3, element SMUX).

8. Alidina has not explicitly taught wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread. However, Alidina has taught an accumulation register is selected from a plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30). Wilson has taught multi-threading requires having several copies of resources, including registers, to preserve the context of each thread (Wilson column 2, lines 46-65). It would have been obvious to a person of ordinary skill in the art to incorporate multiple copies of the accumulation registers for multi-threading as taught by Wilson, because multi-threading increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

9. Referring to claim 2, Alidina has taught a control block operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result corresponding to the selected thread when the operation code corresponds to an accumulate operation (Alidina column 5, lines 8-18).

10. Referring to claim 3, Alidina has taught wherein when the operation code corresponds to an accumulate operation, the control block provides the control information to the selection

block such that the selection block selects a current value stored in the selected accumulation register as the second operand (Alidina columns 1-2, lines 64-5 and Figure 3).

11. Referring to claim 4, Alidina has taught wherein the first operation unit performs an addition operation such that the result of an accumulate operation is a sum of the current value stored in the selected accumulation register and the first operand (Alidina columns 1-2, lines 64-5 and Figure 3).

12. Referring to claim 5, Alidina has taught a second operation unit operably coupled to the first operation unit, wherein the second operation unit is operably coupled to receive a third operand and a fourth operand, wherein the second operation unit combines the third and fourth operands to produce a second operation result, wherein the second operation result is provided to the first operation unit as the first operand (Alidina columns 4-5, lines 26-7 and Figure 3).

13. Referring to claim 6, Alidina has taught wherein the second operation unit performs multiplication operations such that a plurality of multiply and accumulate functions are supported for the plurality of threads by the multi-thread accumulation circuit (Alidina column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3).

14. Referring to claim 7, Alidina has not taught an arbitration module operably coupled to the control block and the second operation unit, wherein the arbitration module receives operation codes from a plurality of thread controllers corresponding to the plurality of threads, wherein the arbitration module determines order of execution of the operation codes received. Wilson has taught an arbitration module operably coupled to the control block and the second operation unit, wherein the arbitration module receives operation codes from a plurality of thread controllers corresponding to the plurality of threads, wherein the arbitration module determines order of

execution of the operation codes received (Wilson column 2, lines 46-65). In regards to Wilson, it inherent that there must be a unit that controls which thread is being executed. It would have been obvious to a person of ordinary skill in the art to incorporate the multi-threading of Wilson, because multi-threading increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

15. Referring to claim 8, Alidina has taught wherein the multi-thread accumulation circuit is included in a vector engine that performs at least one of dot product operations, vector multiply accumulate operations, vector addition operations, and vector multiplication operations (Alidina column 2, lines 57-60).

16. Referring to claim 9, Alidina has taught a memory operably coupled to the selection block, the first operation unit, and the control block, wherein the memory stores the first operation result produced by the first operation unit, wherein contents of the memory are selectively included in the set of potential operands based on a portion of the control information generated by the control block (Alidina column 2, lines 12-19 and 46-48; columns 4-5, lines 26-7; and Figure 3).

17. Referring to claim 10, Alidina has taught wherein at least a portion of the plurality of accumulation registers include a first register section and a second register section, wherein the first register section is used for accumulation operations corresponding to a first set of operation

codes and the second section is used for accumulation operations corresponding to a second set of operation codes (Alidina columns 1-2, lines 54-15 and Figure 1).

18. Referring to claim 12, Alidina has taught a method for performing a plurality of combine and accumulate operations in a multi-thread system that supports a plurality of threads, comprising:

a. Receiving a first set of operands corresponding to a selected thread of the plurality of threads, wherein the first set of operands corresponds to a first accumulation operation for the selected thread (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

b. Combining the first set of operands to produce a first result (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

c. Storing the first result in the selected accumulation register to produce a first accumulated value (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

d. Receiving a second set of operands corresponding to the selected thread, wherein the second set of operands corresponds to a second accumulation operation for the selected thread (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

e. Combining the second set of operands to produce a second result (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

f. Combining the second result with the first accumulated value to produce a second accumulated value (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3)

g. Storing the second accumulated value in the selected register to produce a second accumulated result (Alidina Abstarct, lines 1-4; column 2, lines 46-48; columns 4-5; lines 26-7; and Figure 3).

19. Alidina has not explicitly taught selecting a selected accumulation register from a plurality of accumulation registers based on identity of the selected thread, wherein each accumulation register of the plurality of accumulation registers corresponds to one of the plurality of threads. However, Alidina has taught an accumulation register is selected from a plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30). Wilson has taught multi-threading requires having several copies of resources, including registers, to preserve the context of each thread (Wilson column 2, lines 46-65). It would have been obvious to a person of ordinary skill in the art to incorporate multiple copies of the accumulation registers for multi-threading as taught by Wilson, because multi-threading increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

20. Referring to claim 13, Alidina has taught wherein combining the first set of operands includes combining the first set of operands using a multiplication operation, and wherein the

combining the second set of operations further comprises combining the second set of operands using a multiplication operation (Alidina column 2, lines 46-48l columns 4-5, lines 26-7; and Figure 3).

21. Referring to claim 14, Alidina has taught wherein combining the second result with the first accumulated value further comprises combining the second result with the first accumulated value using an addition operation such that a multiply and accumulate operation for the first and second sets of operands is achieved (Alidina column 2, lines 46-65).

22. Referring to claim 15, Alidina has taught the method comprises:

a. Receiving subsequent sets of operands corresponding to the selected thread ~~corresponding~~ corresponding to subsequent accumulation operations for the selected thread (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3);

b. For each subsequent set of operands:

i. Combining the subsequent set of operands to produce a subsequent result (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

ii. Combining the subsequent result with a current value stored in the selected accumulation register to produce a subsequent accumulated result (Alidina Abstract, lines 1-4; columns 1-2, lines 64-5; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

iii. Storing the subsequent accumulated result in the selected accumulation register such that the current value stored in the selected accumulation

register is updated (Alidina Abstract, lines 1-4; columns 1-2, lines 64-5; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3).

23. Referring to claim 16, Alidina has not taught performing combination operations corresponding to at least one additional thread of the plurality of threads subsequent to combining the first set of operands and prior to combining the second set of operands. Wilson has taught performing combination operations corresponding to at least one additional thread of the plurality of threads subsequent to combining the first set of operands and prior to combining the second set of operands. (Wilson column 2, lines 46-65). It would have been obvious to a person of ordinary skill in the art to incorporate the multi-threading of Wilson, because multi-threading increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

24. Referring to claim 17, Alidina has taught a multi-thread multiply and accumulate circuit, comprising:

a. A multiplier operably coupled to the arbitration module, wherein the multiplier combines a set of operands corresponding to each command code being executed to produce a product corresponding to a selected thread from which the command code being executed originated (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

b. An adder operably coupled to the multiplier, wherein the adder combines the product of the multiplier with a second operand that is received to produce a sum corresponding to selected thread (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

c. A plurality of accumulation registers operably coupled to the adder, wherein each of the plurality of accumulation registers corresponds to one of the plurality of threads (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3)

d. A selection block operably coupled to the plurality of accumulation registers and the adder, wherein the selection block selects the second operand from a set of potential operands based on control information derived from the command code being executed, wherein the set of potential operands includes values stored in each of the plurality of accumulation registers (Alidina column 4, lines 63-66 and Figure 3, element SMUX).

25. Alidina has not explicitly taught wherein a selected accumulation register that corresponds to the selected thread stores the sum corresponding to the selected thread. However, Alidina has taught an accumulation register is selected from a plurality of accumulation registers (Alidina Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3, element 30). Wilson has taught multi-threading requires having several copies of resources, including registers, to preserve the context of each thread (Wilson column 2, lines 46-65). It would have been obvious to a person of ordinary skill in the art to incorporate multiple copies of the accumulation registers for multi-threading as taught by Wilson, because multi-threading

increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

26. In addition, Alidina has not explicitly taught an arbitration module that receives command codes corresponding to a plurality of threads, wherein at least a portion of the command codes correspond to multiply and accumulate operations, wherein the arbitration module determines an order of execution of the command codes. However, Alidina has taught a control means corresponding to command codes (Alidina column 5, lines 8-18). Wilson has taught multi-threading with separate resources, including control resources, for each thread (Wilson column 2, lines 46-65). In regards to Wilson, it inherent that there must be a unit that controls which thread is being executed. It would have been obvious to a person of ordinary skill in the art to incorporate the multi-threading of Wilson, because multi-threading increases speed by allowing the processor to run other procedures while waiting for a longer background operations, such as accessing slower memory, to complete. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multi-threading of Wilson in the device of Alidina to increase speed and decrease processor idle time.

27. Referring to claim 18, Alidina has taught wherein the set of potential operands includes at least one additional operand, wherein the at least one additional operand is at least one of a constant, a state variable, and data stored in a memory structure as a result of previous operations

performed by the circuit (Alidina column 2, lines 12-19 and 46-48; columns 4-5, lines 26-7; and Figure 3).

28. Referring to claim 19, Alidina has taught wherein at least a portion of the plurality of accumulation registers include a first register section and a second register section, wherein the first register section is used for accumulation operations corresponding to a first set of operation codes and the second section is used for accumulation operations corresponding to a second set of operation codes (Alidina columns 1-2, lines 54-15 and Figure 1).

29. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alidina et al., U.S. Patent Number 6,446,193 (herein referred to as Alidina) in view of Wilson, U.S. Patent Number 5,896,517 (herein referred to as Wilson) as applied to claims 10 and 19 above, and further in view of Berkaloff, U.S. Patent Number 5,673,377 (herein referred to as Berkaloff).

30. Referring to claim 11, Alidina has not explicitly taught wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics primitives. However, Alidina has taught that DSP processors are optimal for certain graphical and audio operations requiring multiplication, accumulation, and other processor intensive operations. Berkaloff has taught that diffuse and specular color information is needed for 3-D graphical calculations (Berkaloff column 1, lines 17-59). It would have been obvious to one of ordinary skill in the art to incorporate the color information of Berkaloff, because it is needed in the calculations to create effective images. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the color information of Berkaloff in the device of Alidina.

31. Referring to claim 20, Alidina has not explicitly taught wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics primitives. However, Alidina has taught that DSP processors are optimal for certain graphical and audio operations requiring multiplication, accumulation, and other processor intensive operations. Berkaloff has taught that diffuse and specular color information is needed for 3-D graphical calculations (Berkaloff column 1, lines 17-59). It would have been obvious to one of ordinary skill in the art to incorporate the color information of Berkaloff, because it is needed in the calculations to create effective images. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the color information of Berkaloff in the device of Alidina.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Aono et al., U.S. Patent Number 5,278,781, has taught a multiply-accumulate unit.

b. Harrison et al., U.S. 5,522,085, has taught a dual multiply-accumulate unit with multiple accumulators.

c. Adelman et al., U.S. Patent Number 5,598,362, has taught multiply-accumulate units with multiple accumulator registers.

d. Pechanek et al., U.S. Patent Number, 6,343,356, has taught multiply-accumulate units associated with register files.

e. Fox, U.S. Patent Number 6,340,972, has a diffuse and specular calculators attached to an accumulator.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

35. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

March 9, 2003

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SUPERVISORY PATENT EXAMINER
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